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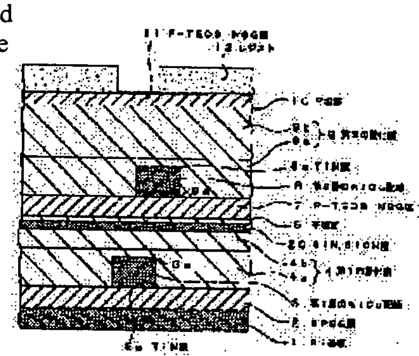
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent an erroneous short circuit and a breakdown-strength defect from being generated in a connecting operation using a borderless contact hole by a method wherein a hard-to-etch layer which is composed of SiN, SiON, SiC, SiCN or the like containing N or C is formed in the intermediate part of an insulating layer at the lower layer of a metal interconnection.
SOLUTION: A borophosphosilicate glass film 2 which constitutes an insulating film is formed on an Si substrate 1, and a first-layer AlCu interconnection 3 is micromachined by a dry-etching operation so as to be formed on it. A first oxide film 4 is formed on the AlCu interconnection 3 and the borophosphosilicate glass film 2. After that, the first oxide film 4 is polished, a flat face 5 is formed, ions are implanted into the whole face of a wafer from the flat face 5, and a hard-to-etch layer 20 which is composed of SiN is formed. In addition, an NSG film 7 and a second-layer AlCu interconnection 8 are micromachined by a dry-etching operation so as to be formed on the flat face 5.



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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by preparing the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. which contain N or C in the interstitial segment of the insulating layer of a lower layer of a metal wiring in the semiconductor device which was made to perform a multilevel-metal wiring on a semiconductor substrate.
[Claim 2] The semiconductor device characterized by using as the etching stop layer in the case of etching of the contact hole of a high aspect ratio the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. containing the aforementioned N or C in a semiconductor device according to claim 1.
[Claim 3] It is the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. containing the aforementioned N or C in a semiconductor device according to claim 1 C+ Or N+ Semiconductor device characterized by forming by carrying out an ion implantation.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention is applied to for example, VLSI equipment, and relates to a suitable semiconductor device.
[0002]
[Description of the Prior Art] In order to attain reduction of each configuration element in accordance with high integration of a semiconductor device in recent years, the continuation **** borderless contacting method which used the contact hole which does not have the degree of additional coverage in the interconnection between each of this configuration element is being used.
[0003] When processing a contact hole by this borderless contacting method, they are C4 F8/CO/Ar, CHF3 / CO/Ar, C4 F8 / CO/Ar / O2. Magnetron reactive ion etching (magnetron RIE) using the mixed gas of a grade is used.
[0004] In this magnetron RIE, since manipulation conditions are set up so that good mu-loading effect may be obtained with the selection ratio of a high opposite resist, opposite TiN, and TiW and W, the borderless contact hole with the high aspect ratio with the good (theta= 88 degrees - 90 degrees) angle control with few dimension conversion differences can be obtained.
[0005]
[Problem(s) to be Solved by the Invention] Since mu-loading effect to the contact hole of a detailed path (phi= 0.50 micrometers or less) is raised in this magnetron RIE, More than advance (omission nature) of etching of the oxide film which constitutes the insulator layer of the fraction which forms a borderless contact hole expected, are good. For example, as shown in drawing 7 , when it is going to obtain the contact hole to the metal wiring (AlCu wiring) 8, the phenomenon in which the pars basilaris ossis occipitalis of this contact hole 13a reaches to the lower layer of this AlCu wiring 8 is seen (a metal wiring lower layer should dig).
[0006] By this, the shunt, a pressure-proof failure, etc. between multilayer interconnections occurred, and there was un-arranging [which cannot acquire a good electrical property].
[0007] Furthermore, with reference to drawing 7 , it attaches inconvenient [this former] and explains. Si substrate by which, as for 1, accumulation formation of the transistor etc. was carried out in drawing 7 , the boron phosphorus ********** glass (BPSG) layer by the reflow from which 2 constitutes an insulator layer, The titanium night ****** (TiN) layer with which 3 put the 1st-layer AlCu wiring and 3a on the upper and lower sides of this 1st-layer AlCu wiring 3, 4 is P-TEOS formed by the plasma CVD which constitutes a layer insulation layer. NSG layer and O3-TEOS The 1st oxide film which consists of two-layer [with NSG layer], 7 is P-TEOS. The insulator layer which consists of NSG layer, and 8 The 2nd-layer AlCu wiring, 9 is TiN layer which put 8a on the upper and lower sides of this 2nd-layer AlCu wiring, and P-TEOS which constitutes a layer insulation layer. NSG layer and O3-TEOS The 2nd oxide film which consists of two-layer [with NSG layer], 11 is P-TEOS. The insulator layer which consists of NSG layer, and 14 are TiN layers which put the 3rd-layer AlCu wiring and 14a on the upper and lower sides of this 3rd-layer AlCu wiring 14.
[0008] In the example of **** view 7 to connect the 2nd-layer AlCu wiring 8 and the 3rd-layer AlCu wiring 14 When borderless contact hole 13a is formed by this magnetron RIE As it is good more than advance (omission nature) of this etching expected, and the base of this contact hole 13a shows in drawing 7 the connection formed by CVD and the etchback method when it had reached to the 1st-layer AlCu wiring 3 -- a conductor (for example, W plug) 13 produces un-arranging which also incorrect-short-circuits the 1st-layer AlCu wiring 3]
[0009] It incorrect-connects too hastily or this invention aims at a pressure-proof failure etc. being made not to occur, when it is made to connect by the borderless contact hole in view of ******.
[0010]
[Means for Solving the Problem] this invention semiconductor device prepares the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. which contain N or C in the interstitial segment of the insulating layer of a lower layer of a metal wiring on a semiconductor substrate in the semiconductor device which was made to perform a multilevel-metal wiring.
[0011] Since it becomes the etching stop layer at the time of forming the contact hole of a high aspect ratio in magnetron RIE, when it is made to connect by this borderless contact hole, the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. containing N or C by **** and this invention is between multilevel-metal wirings, the incorrect shunt is not

produced or a pressure-proof failure etc. does not generate it.
[0012]
[Embodiments of the Invention] With reference to view 1 - view 3 , an example of the gestalt of operation of this invention semiconductor device is explained below according to the example of a manufacture. In this drawing 1 - view 3 , the same sign is attached and shown in the fraction corresponding to drawing 7 .
[0013] In this example, as first shown in drawing 2 , a transistor etc. forms the boron phosphorus ********** glass (BPSG) layer 2 by the reflow which constitutes an insulator layer on the Si substrate 1 by which accumulation formation was carried out. On this BPSG layer 2, micro processing of the 1st-layer AlCu wiring 3 which made this BPSG layer 2 the substratum is carried out by dry etching, and it is formed. In this case, it carries out as [put / TiN layer 3a / on the vertical side of this 1st-layer AlCu wiring 3]. The thickness of this 1st-layer AlCu wiring 3 is set to about 500nm.
[0014] P-TEOS formed by the plasma CVD method on this AlCu wiring 3 and BPSG layer 2 of the 1st layer NSG layer 4a and O3-TEOS The 1st oxide film 4 which constitutes the layer insulation layer which consists of two-layer [of NSG layer 4b] is formed.
[0015] Then, this 1st oxide-film 4 top is ground by the CMP method, suppose that it is flat, and the flat side 5 is formed. In this case, the thickness of this 1st oxide film 4 is set to about 900nm.
[0016] In this example, it forms as a difficulty etching layer by the plasma CVD method on this flat side 5, the SiN layer 6, i.e., the P-SiN layer, which are 200nm or less in thickness, and a 100nm insulator layer. As conditions which form this P-SiN layer 6, it considered as NH3 / SiH4 / N2 =300/100/3000sccm, 4.0Torr, 600W, and 400 degrees C, and parallel monotonous type plasma CVD equipment was used.
[0017] Next, they are 200nm or less in thickness, and 100nm P-TEOS by the plasma CVD method on this P-SiN layer 6. The NSG layer 7 is formed. This P-TEOS As conditions which form the NSG layer 7, it considered as O2 / TEOS=500/900sccm, 8.0Torr, 800W, and 400 degrees C, and parallel monotonous type plasma CVD equipment was used.
[0018] This P-TEOS It is this P-TEOS on the NSG layer 7. Micro processing of the 2nd-layer AlCu wiring 8 which made the NSG layer 7 the substratum is carried out by dry etching, and it is formed. In this case, it carries out as [put / TiN layer 8a / on the vertical side of this 2nd-layer AlCu wiring 8]. The thickness of this 2nd-layer AlCu wiring 8 is set to about 500nm.
[0019] This 2nd-layer AlCu wiring 8 and P-TEOS P-TEOS formed by the plasma CVD method on the NSG layer 7 NSG layer 9a and O3-TEOS The 2nd oxide film 9 which constitutes the layer insulation layer which consists of two-layer [of NSG layer 9b] is formed.
[0020] Then, this 2nd oxide-film 9 top is ground by the CMP method, suppose that it is flat, and the flat side 10 is formed. In this case, the thickness of this 2nd oxide film 9 is set to about 900nm.
[0021] They are 200nm or less in thickness, and 100nm P-TEOS by the plasma CVD method on this flat side 10. The NSG layer 11 is formed.
[0022] This P-TEOS It carries out as [form / the resist 12 of magnetron RIE by which the pattern of the borderless contact hole of a predetermined number was formed on the NSG layer 11].
[0023] Next, this resist 12 is used and etching of the borderless contact hole by magnetron RIE is carried out. Here, 1.5-micrometer etching of a high aspect ratio is carried out by depth conversion including a part for the over etching of the thickness of the deepest layer insulation layer. By optimizing etching conditions, it is carrying out as [acquire / a good property / to mu-loading effect, the selection ratio for a resist, the selection ratio for TiN, an angle control, etc.].
[0024] The conditions of this etching are C4 F8/CO/Ar/O2 =12/100/200/5sccm, 6.0Pa, 1600W, 20 degrees C, and P-TEOS. It ****s at the selection ratio for TiN 25, more than mu-loading-effect =85%, and theta= 88 degrees or more of angle controls NSG=450nm/min**4.8%.
[0025] In this case, in contact hole 13a of the shallowest layer insulation thickness, if the base of contact hole 13a reaches in depth of 1.1 micrometers (bottom 100nm of the 2nd-layer AlCu wiring 8), as shown in drawing 3 , the P-SiN layer 6 will be exposed to the base of this contact hole 13a, and advance of this etching will be prevented. This is C4 F8/CO/Ar / O2 like common knowledge. SiO2 to SiN It is for the device of high selection-ratio etching to work (refer to JP,6-132252,A).
[0026] Moreover, P-TEOS which is the oxide film of the substratum of the 2nd-layer AlCu wiring 8 in shallow contact hole 13a of a layer insulation thickness in order that an etching stop with the P-SiN layer 6 may work **** of NSG7 becomes complete in a fixed depth (this example under the 2nd-layer AlCu wiring 8 100nm). In deep contact hole 13a, in order to be applied to the thickness of a layer insulation layer by the amount of over etching, contact hole 13a which is a high aspect ratio punctures.
[0027] Then, a resist 12 is removed as shown in drawing 3 by known technique. next, this contact hole 13a -- CVD and the etchback method -- or CVD and the CMP method -- connection -- a conductor (for example, W plug) 13 is formed
[0028] it is shown in drawing 1 -- as -- connection of this contact hole 13a -- it connects with the top of a conductor 13 electrically, and micro processing of the 3rd-layer AlCu wiring 14 is carried out by dry etching, and it is formed In this case, it carries out as [put / TiN layer 14a / on the vertical side of this 3rd-layer AlCu wiring 14]. The thickness of this AlCu wiring 14 is set to about 500nm.
[0029] Since the P-SiN layer 6 is used as the etching stop layer while borderless contact hole 13a of a high aspect ratio can be formed good, since mu-loading effect is improved according to this example, when the 3rd-layer AlCu wiring 14 and the 2nd-layer AlCu wiring 8 are connected using this borderless contact hole 13a, the incorrect shunt is not produced, or a pressure-proof failure etc. does not occur.

[0030] That is, according to this example, since between the 1st-layer AlCu wiring 3 and the bases of borderless contact hole 13a is set as 400nm or more, about [that the incorrect shunt does not arise] and the pressure-proofing between layers is also secured, and there are profits which can acquire a good electrical property.
[0031] Therefore, when this example is applied to VLSI equipment, there are profits which can obtain the VLSI equipment with a good reliability for a high quality.
[0032] In addition, although the above-mentioned example took lessons from the example which used the SiN layer 6 (P-SiN layer by plasma CVD) and was stated as a difficulty etching layer, of course, the thin film containing N, such as SiON and SiOFN, can instead be used.
[0033] Moreover, although plasma CVD equipment was used for forming membranes in the above-mentioned example, of course, high-density CVD systems, such as efficient consumer response (Electoron Cyclotron Resonance) CVD system, a helicon wave CVD system, and ICP (Inductively Coupled Plasma) CVD system, can instead be used.
[0034] Next, with reference to drawing 4 , the drawing 5 , and the drawing 6 , it explains per other examples of the gestalt of operation of this invention. In this drawing 4 , the drawing 5 , and the drawing 6 , the same sign is attached and shown in the fraction corresponding to drawing 1 , the drawing 2 , and the drawing 3 .
[0035] In this example, as first shown in drawing 4 , a transistor etc. forms the boron phosphorus ********** glass (BPSG) layer 2 by the reflow which constitutes an insulator layer on the Si substrate 1 by which accumulation formation was carried out. On this BPSG layer 2, micro processing of the 1st-layer AlCu wiring 3 which made this BPSG layer 2 the substratum is carried out by dry etching, and it is formed. In this case, it carries out as [put / TiN layer 3a / on the vertical side of this 1st-layer AlCu wiring 3]. The thickness of this 1st-layer AlCu wiring 3 is set to about 500nm.
[0036] P-TEOS formed by the plasma CVD method on this AlCu wiring 3 and BPSG layer 2 of the 1st layer NSG layer 4a and O3-TEOS The 1st oxide film 4 which constitutes the layer insulation layer which consists of two-layer [of NSG layer 4b] is formed.
[0037] Then, this 1st oxide-film 4 top is ground by the CMP method, suppose that it is flat, and the flat side 5 is formed. In this case, the thickness of this 1st oxide film 4 is set to 500nm - 900nm.
[0038] Then, it sets to this example and is N+ from this flat side 5. An ion implantation is carried out all over a wafer, and the difficulty etching layer 20 which consists of SiN is formed. This N+ that carried out the ion implantation Mean projection range Rp 100nm or less is suitable from this flat side 5. This mean projection range Rp Standard deviation deltaRp Since it is about [**30nm], the layer mixed by high concentration is formed in about 60nm (although the mixing layer after injection is amorphous, it polycrystal-izes by heating under membrane formation of the layer mesenteriolum, and SiN, SiON mixed crystal, etc. generate.).
[0039] This N+ Ion-implantation conditions are acceleration energy 100KeV, N+=1E16cm2, and room temperature injection.
[0040] Next, it is 100nm P-TEOS by the plasma CVD method on this flat side 5. The NSG layer 7 is formed. This P-TEOS As conditions which form the NSG layer 7, it considered as O2 / TEOS=500/900sccm, 8.0Torr, 800W, and 400 degrees C, and parallel monotonous type plasma CVD equipment was used.
[0041] This P-TEOS It is this P-TEOS on the NSG layer 7. Micro processing of the 2nd-layer AlCu wiring 8 which made the NSG layer 7 the substratum is carried out by dry etching, and it is formed. In this case, it carries out as [put / TiN layer 8a / on the vertical side of this 2nd-layer AlCu wiring 8]. The thickness of this 2nd-layer AlCu wiring 8 is set to about 500nm.
[0042] This 2nd-layer AlCu wiring 8 and P-TEOS P-TEOS formed by the plasma CVD method on the NSG layer 7 NSG layer 9a and O3-TEOS The 2nd oxide film 9 which constitutes the layer insulation layer which consists of two-layer [of NSG layer 9b] is formed.
[0043] Then, this 2nd oxide-film 9 top is ground by the CMP method, suppose that it is flat, and the flat side 10 is formed. In this case, the thickness of this 2nd oxide film 9 is set to 500nm - 900nm. They are 200nm or less in thickness, and 100nm P-TEOS by the plasma CVD method on this flat side 10. The NSG layer 11 is formed.
[0044] This P-TEOS It carries out as [form / the resist 12 of magnetron RIE in which the pattern which forms the borderless contact hole of a predetermined number on the NSG layer 11 was formed].
[0045] Next, this resist 12 is used and etching of the borderless contact hole by magnetron RIE is carried out. Here, 1.5-micrometer etching of a high aspect is carried out by depth conversion including a part for the over etching of the thickness of the deepest layer insulation layer. By optimizing this etching condition, it is carrying out as [acquire / a good property / to mu-loading effect, the selection ratio for a resist, the selection ratio for TiN, an angle control, etc.].
[0046] This etching condition is C4 F8/CO/Ar/O2 =12/100/200/5sccm, 6.0Pa, 1600W, 20 degrees C, and P-TEOS. It considers as the selection ratio for TiN 25, more than mu-loading-effect =85%, and theta= 88 degrees or more of angle controls NSG=450nm/min**4.8%.
[0047] In this case, in contact hole 13a of the shallowest layer insulation layer, if the base of this contact hole 13a reaches in depth of 1.1 micrometers (bottom 100nm of the 2nd-layer AlCu wiring 8), as shown in drawing 5 , the difficulty etching layer 20 of SiN and SiON will be exposed to the base, and advance of this etching will be prevented. This is C4 F8 / Co/Ar / O2 like common knowledge. SiO2 to SiN It is for the device of high selection-ratio etching to work (refer to JP,6-132252,A).
[0048] Moreover, in order that an etching stop in the difficulty etching layer 20 of SiN and SiON may work in shallow contact hole 13a of the thickness between layers, it is a depth (it becomes complete by about 200nm under AlCu wiring) with fixed **** of the oxide film of the substratum of a wiring. since it is applied to the thickness of a layer insulation layer by the

amount of over etching in deep contact hole 13a -- high -- an aspect contact hole punctures
[0049] Then, a resist 12 is removed as shown in drawing 5 by known technique. next, this contact hole 13a -- CVD and the etchback method -- or CVD and the CMP method -- connection -- a conductor (for example, W plug) 13 is formed
[0050] it is shown in drawing 6 -- as -- connection of this contact hole 13a -- it connects with the top of a conductor 13 electrically, and micro processing of the 3rd-layer AlCu wiring 14 is carried out by dry etching, and it is formed In this case, it carries out as [put / TiN layer 14a / on the vertical side of this 3rd-layer AlCu wiring 14]. The thickness of this AlCu wiring 14 is set to about 500nm.
[0051] Since the difficulty etching layer 20 of SiN and SiON is used as the etching stop layer while borderless contact hole 13a of a high aspect ratio can be formed good, since mu-loading effect is improved according to this example When **** of a contact hole is stopped by this and the 3rd-layer AlCu wiring 14 and the 2nd-layer AlCu wiring 8 are connected using this borderless contact hole 13a, the incorrect shunt is not produced, or a pressure-proof failure does not occur.
[0052] Moreover, according to this example, it is N+. The difficulty etching layer 20 of arbitrary SiNs and SiON can be formed by setting the injection conditions of ion as a desired value.
[0053] In addition, it sets in the above-mentioned example and is N+. Although lessons was taken from the example which poured in ion and formed the difficulty etching layer of SiN and SiON and being stated, it is instead C+. Ion is poured in, and it is good also as a difficulty etching layer of SiC, and is C+. Ion and N+ Even if it forms the difficulty etching layer of SiCN by double injection of ion, it can be understood easily that the same operation effect as **** is acquired.
[0054] This C+ The examples of the conditions of an ion implantation are 100KeVs, C+=1E16cm2, and room temperature injection.
[0055] Moreover, this invention of the ability of various configurations to take is natural, without deviating from the summary of this invention, without restricting to the above-mentioned example.
[0056]
[Effect of the Invention] Since according to this invention mu-loading effect is improved, and the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. containing N or C is used as the etching stop layer while the borderless contact hole of a high aspect ratio can be formed good The position of the base of this borderless contact hole is decided, and there are profits which do not produce the incorrect shunt when connecting between multilevel-metal wirings by this borderless contact hole, or a pressure-proof failure etc. does not generate.
[0057] Therefore, according to this example, it is quality and there are profits which can obtain semiconductor devices, such as a VLSI element with a good reliability.

[Translation done.]

* NOTICES *

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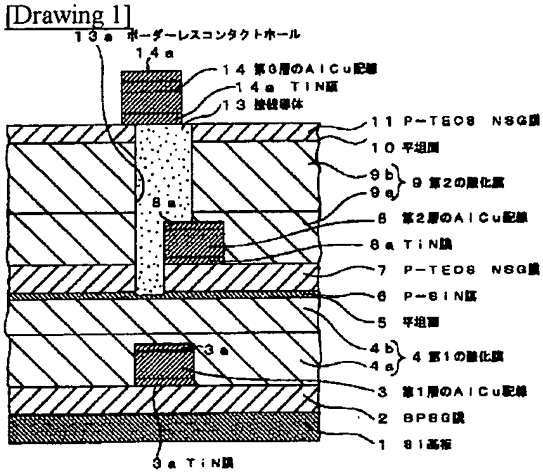
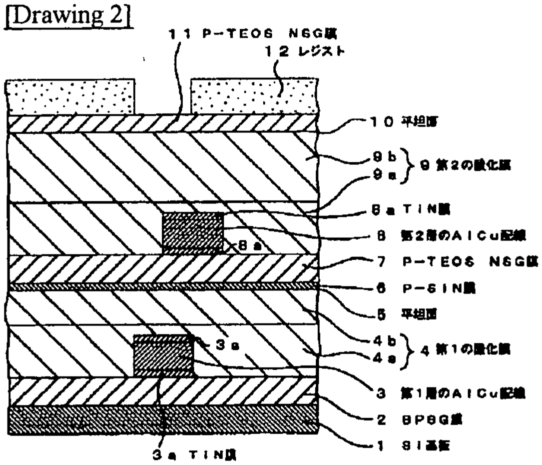
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

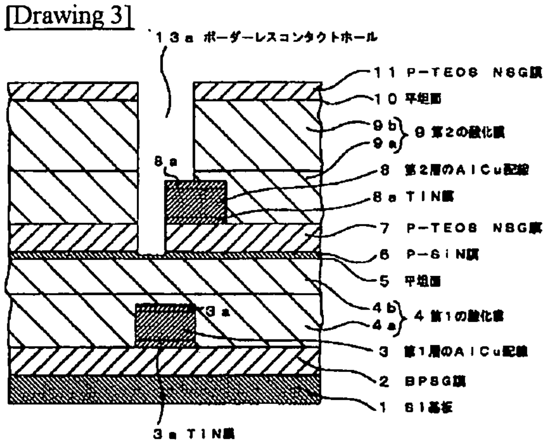
[Drawing 1]



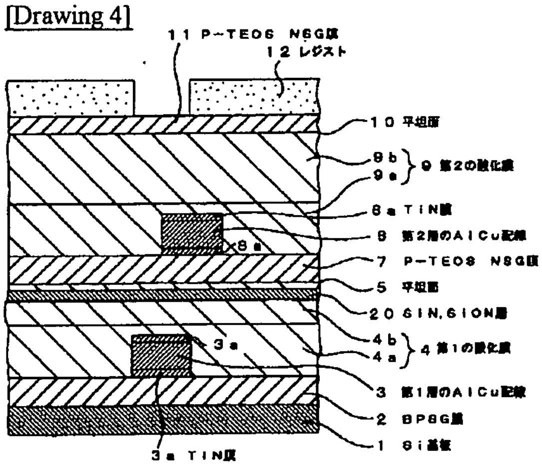
[Drawing 2]



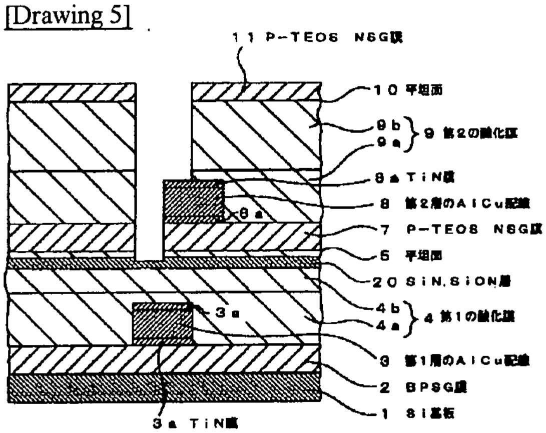
[Drawing 3]



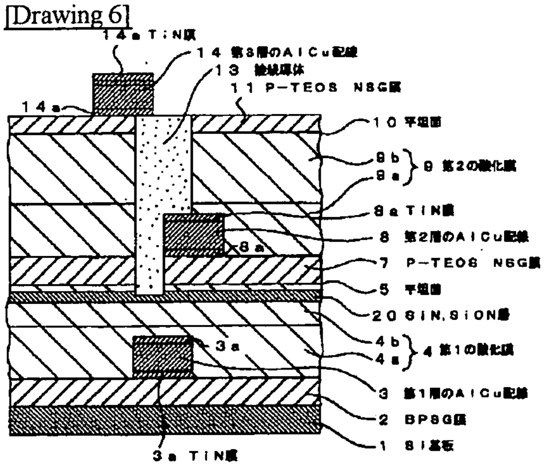
[Drawing 4]



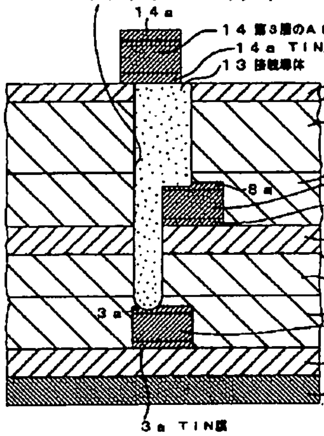
[Drawing 5]



[Drawing 6]



[Drawing 7]



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